IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yi Ding		
Assignee:	ProMOS Technologies, Inc.		
Title:	Nonvolatile Memory Cell With Multiple Floating Gates Formed After The Select Gate		
Serial No.:	10/631,941	Filing Date:	July 30, 2003
U.S. Patent No.:	7,169,667	Issue Date:	January 30, 2007
Examiner:	Lindsay Jr., Walter Lee	Group Art Unit:	2812
Docket No.:	M-15171 US	Confirmation No.:	1763

San Jose, California
March 20, 2007

Attn: Certificate of Corrections Branch
Commissioner For Patents
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Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Sir:

Please enter the enclosed Certificate of Correction (5 pages) in the above patent.

The errors sought to be corrected were made by the Patent and Trademark Office. Thus, no fee is believed to be required for the Certificate of Correction pursuant to 37 C.F.R. § 1.322. If however a fee is required, please charge Deposit Account No. 50-2257. The undersigned can be contacted at (408) 392-9250 with any questions regarding this request.

Certificate of Transmission: I hereby certify that this correspondence is being transmitted to the United States Patent and Trademark Office (USPTO) via the USPTO's electronic filing system on March 20, 2007.

Michael Shenker — Attorney for Applicant(s)
3-20-07 — Date of Signature

Respectfully submitted,

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PTO/SB/44 (04-05)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,169,667 B2

APPLICATION NO.: 10/631,941

ISSUE DATE : January 30, 2007

INVENTOR(S) : Yi Ding

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

After column 12, line 59, please insert the following claims:

--11. The method of Claim 1 wherein the nonvolatile memory cell is part of an array of nonvolatile memory cells, each memory cell of the array having conductive floating gates FG1 and FG2 and a first conductive gate;

wherein the method comprises, before the operation (1), performing the following operation:

(a) forming one or more substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (1) comprises:

(b) forming one or more conductive lines G1, each conductive line G1 overlying at least one active area, wherein each first conductive gate comprises a portion of a line G1;

wherein the operation (2) comprises:

(c) forming a layer ("FG layer") over the first conductive lines and the substrate isolation regions, wherein each of the floating gates FG1, FG2 of each memory cell comprises a portion of the FG layer;

(d) partially removing the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each conductive line G1.

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(continued)

12. The method of Claim 11 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

13. The method of Claim 12 wherein each substrate isolation region traverses the memory array, and each conductive line G1 crosses over plural substrate isolation regions.

14. The method of Claim 11 wherein the top surface of each line G1 is planar but the bottom surface of each line G1 goes up and down over the substrate isolation regions.

15. The method of Claim 11 further comprising, before forming the FG layer, forming a dielectric over sidewalls of each conductive line G1 to insulate the conductive lines G1 from the floating gates.

16. The method of Claim 15 wherein each memory cell further comprises two second conductive gates insulated from the first conductive gate and the floating gates FG1 and FG2, and the method further comprises:

(e) after the operation (d), forming a dielectric D1 over the FG layer;

(f) forming a layer G2 over the dielectric D1, wherein each second conductive gate comprises a portion of the layer G2;

(g) partially removing the layer G2 and the FG layer to form the floating gates and to form from the layer G2 one or more conductive lines for the second conductive gates, wherein each second conductive gate comprises a portion of a conductive line formed from the layer G2.

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(continued)

17. The method of Claim 16 wherein in the operation (f), the layer G2 is formed to have a portion P1 protruding above each conductive line G1; and

the operation (g) comprises:

(g1) forming a layer L1 over the layer G2 such that the protruding portions P1 of the layer G2 are exposed and not completely covered by the layer L1;

(g2) at least partially removing the protruding portions P1 of the layer G2 to form a gap in the layer G2 over each line G1, wherein at a conclusion of this removing operation a portion of the layer G2 remains covered by the layer L1;

(g3) forming a layer L2 on the layer G2 adjacent to the gaps; and

(g4) removing at least parts of the layers L1 and G2 selectively to the layer L2.

18. The method of Claim 17 wherein the operation (g1) comprises:

forming the layer L1 over the entire layer G2; and

planarizing the layer L1 to expose the protruding portions P1.

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(continued)

19. The method of Claim 17 wherein the operation (g3) comprises reacting the layer G2 with another material to form the layer L2.

20. The method of Claim 19 wherein the reacting operation comprises oxidation of the layer G2.

21. The method of Claim 19 wherein the reacting operation comprises a chemical reaction of the layer G2 with a metal, and the chemical reaction is followed by removal of non-reacted metal.

22. The method of Claim 17 further comprising, after the operation (g4):

removing the layer L2 to expose an underlying surface of the layer G2; and

reacting the exposed surface of the layer G2 with a conductive material to form a conductive layer on the surface of the layer G2.

23. The method of Claim 22 wherein the conductive layer has a lower resistivity than the layer G2.

24. The method of Claim 22 further comprising, before the reacting operation, forming dielectric on at least portions of sidewalls of the layer G2, wherein the conductive layer is formed selectively on the exposed surface of the layer G2 but not on the dielectric.

25. The method of Claim 22 wherein the reacting operation comprises a reaction with a metal.

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(continued)

26. The method of Claim 22 wherein:

the first conductive gate is part of a first conductive line that provides first conductive gates to a plurality of nonvolatile memory cells;

each of the second conductive gates is part of a second conductive line that provides second conductive gates to said plurality of the memory cells;

the portion P1 and the conductive layer extend along the first conductive line through said plurality of the memory cells, the conductive layer reducing the sheet resistance of the second conductive lines.

27. The method of Claim 22 wherein the memory cell comprises a source/drain region in the semiconductor substrate, and the conductive layer forms on the source/drain region. --

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